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(54) **CIRCUIT AND SYSTEM FOR CONCURRENTLY PROGRAMMING MULTIPLE BITS OF OTP MEMORY DEVICES**

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CPC G11C 17/16; G11C 17/165; G11C 17/143; G11C 11/146; G11C 17/18
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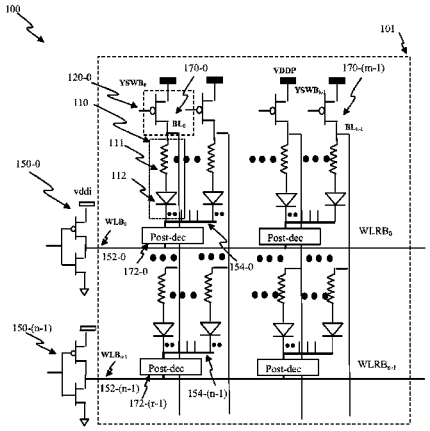
(57) **ABSTRACT**

Circuits and systems for concurrently programming a plurality of OTP cells in an OTP memory are disclosed. Each OTP cell can have an electrical fuse element coupled a program selector having a control terminal. The control terminals of a plurality of OTP cells can be coupled to a plurality of local wordlines, and a plurality of the local wordlines can be coupled to at least one global wordline. A plurality of banks of bitlines can have each bitline coupled to a plurality of the OTP cells via the control terminal of the program selector. A plurality of bank selects can enable turning on the wordlines or bitlines in a bank. A plurality of the OTP cells can be configured to be programmable concurrently into a different logic state by applying voltages to at least one selected global wordline and at least one selected bitline to a plurality of the selected OTP cells in a plurality of banks, if a plurality of banks are enabled.

22 Claims, 8 Drawing Sheets



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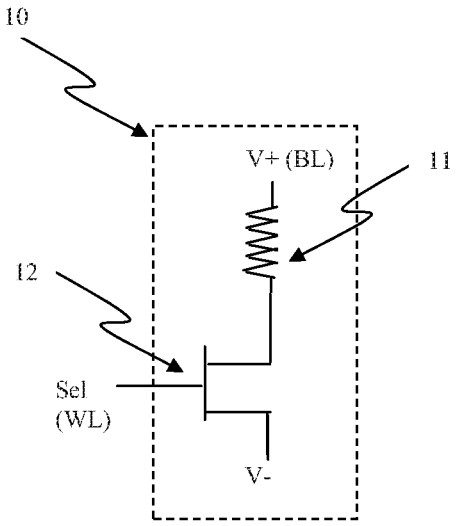

FIG. 1 (prior art)

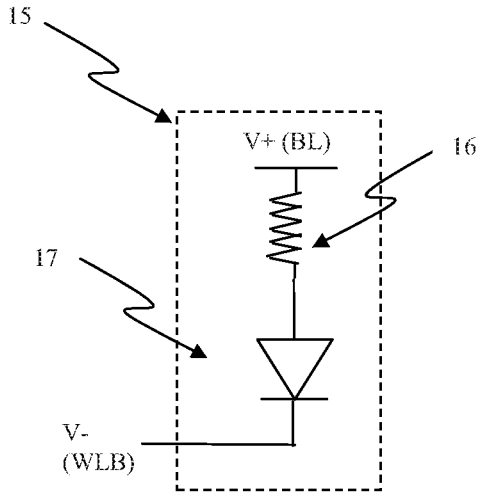

FIG. 2 (prior art)

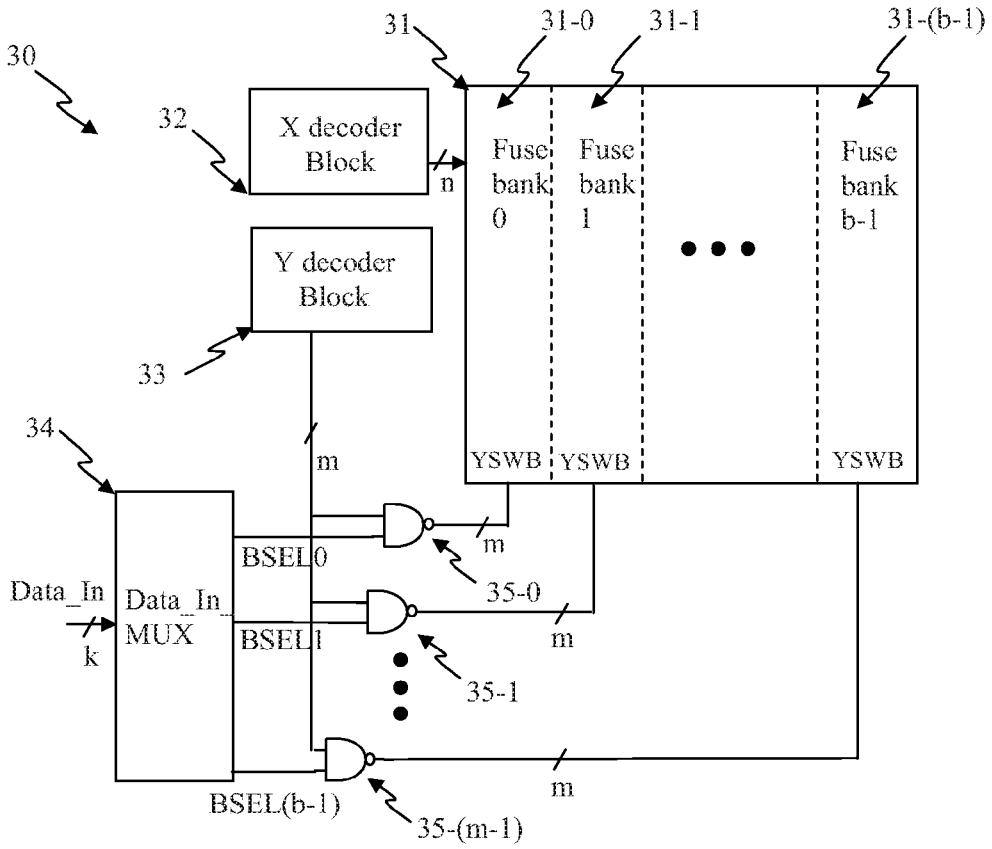
30
31
31-0
31-1
31-(b-1)
32
X decoder Block
n
Fuse bank 0
Fuse bank 1
Fuse bank b-1
Y decoder Block
33
34
m
YSWB
YSWB
YSWB
BSEL0
m
35-0
Data_In
Data_In MUX
k
BSEL1
m
35-1
BSEL(b-1)
m
35-(m-1)

FIG. 3

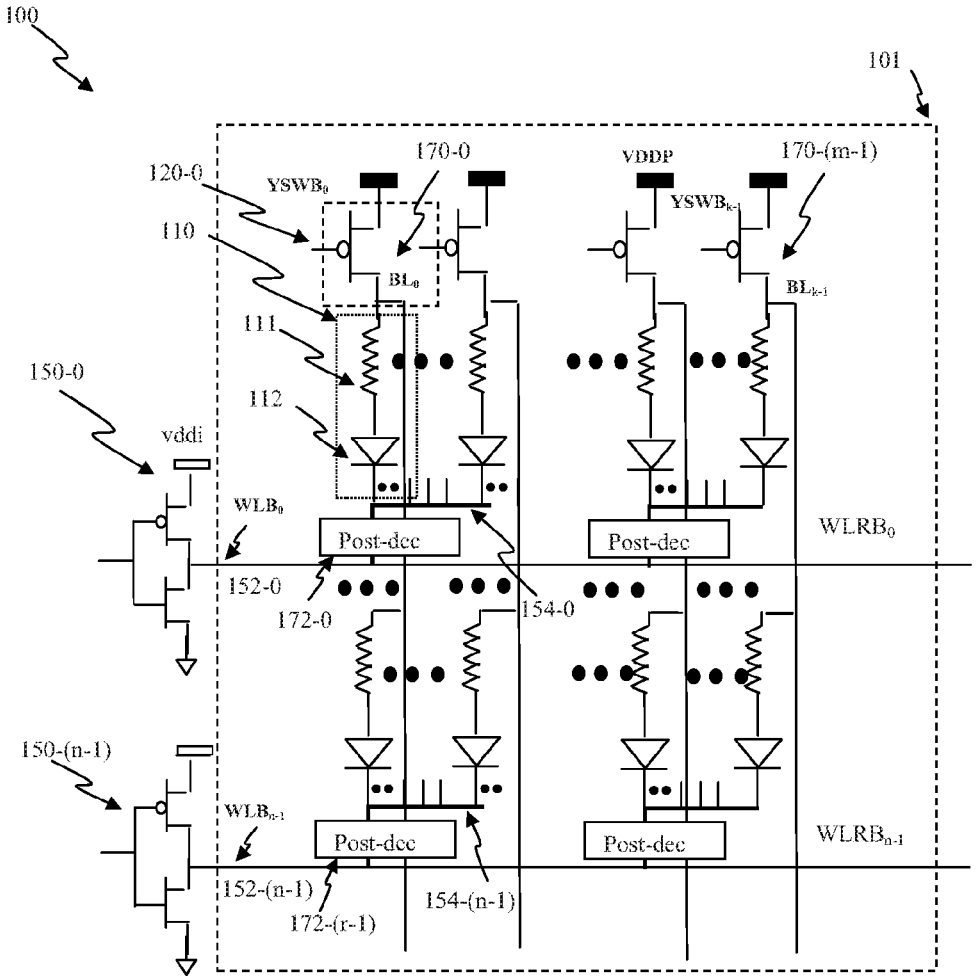
100
101
120-0
110
111
112
150-0
vddi
150-(n-1)
170-0
VDDP
170-(m-1)
YSWB0
YSWBk-1
BL0
BLk-1
WLB0
WLBn-1
Post-dec
Post-dec
Post-dec
Post-dec
WLRB0
WLRBn-1
152-0
172-0
154-0
152-(n-1)
172-(r-1)
154-(n-1)

FIG. 4

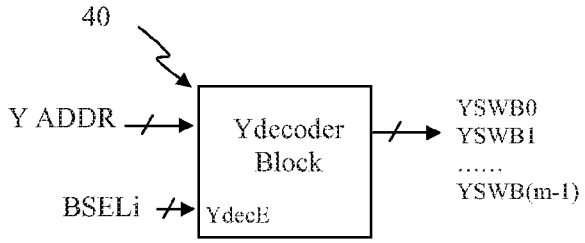
40
Y ADDR
Ydecoder Block
BSELi
YdecE
YSWB0
YSWB1
.....
YSWB(m-1)

FIG. 5(a)

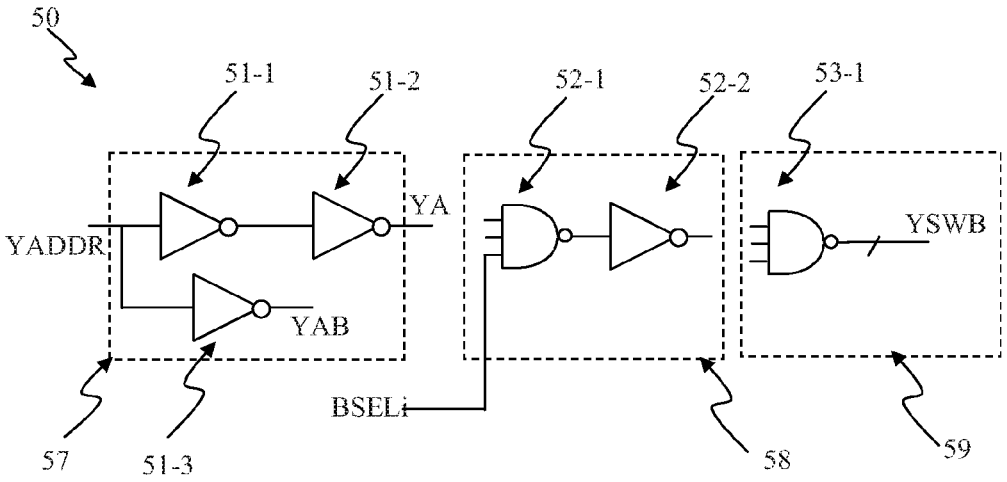
50
51-1
51-2
52-1
52-2
53-1
YA
YADDR
YAB
YSWB
BSELi
57
51-3
58
59

FIG. 5(b)

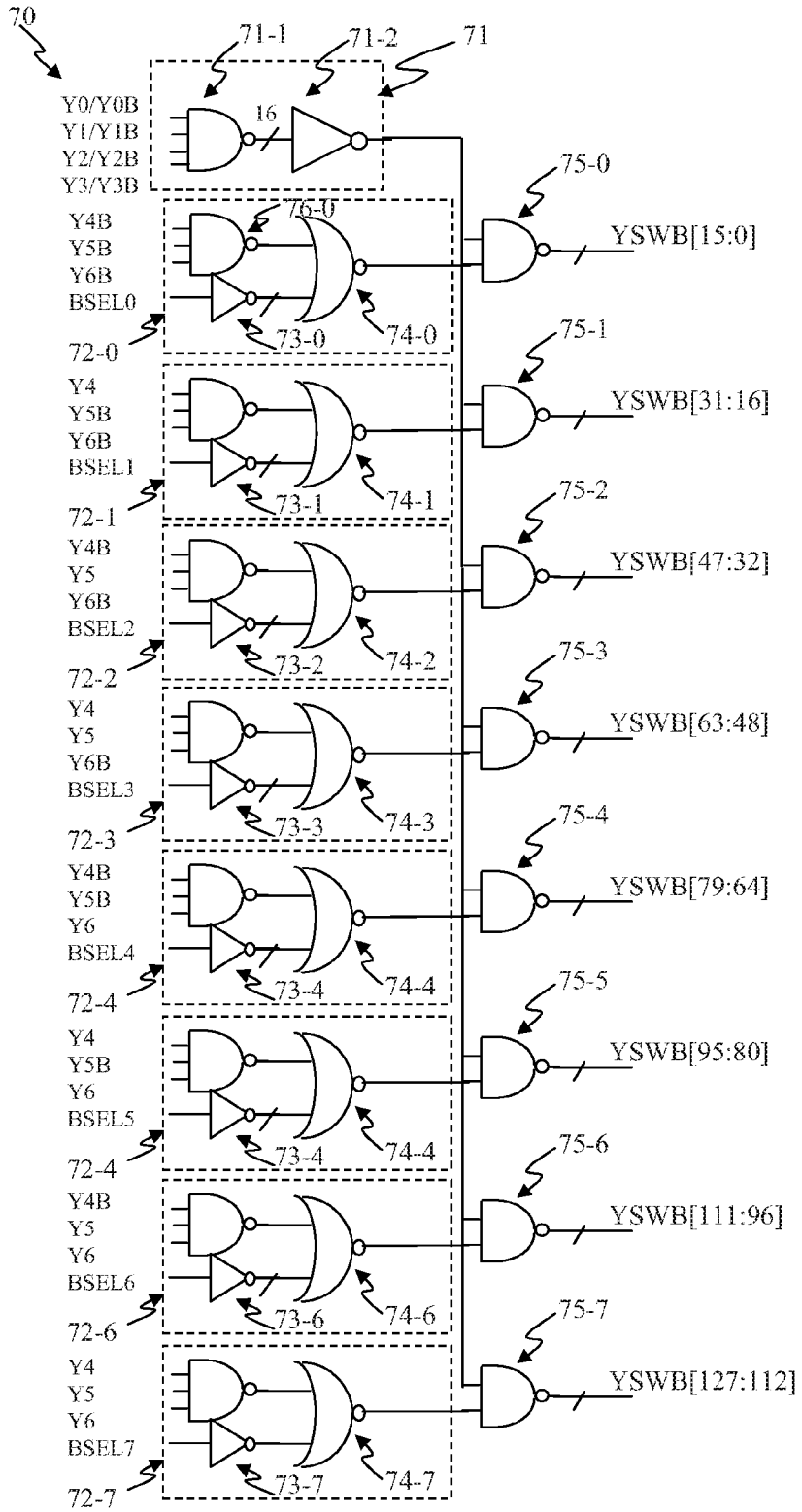
70
71-1
71-2
71
Y0/Y0B
Y1/Y1B
Y2/Y2B
Y3/Y3B
16
75-0
76-0
Y4B
Y5B
Y6B
BSEL0
72-0
73-0
74-0
YSWB[15:0]
75-1
Y4
Y5B
Y6B
BSEL1
72-1
73-1
74-1
YSWB[31:16]
75-2
Y4B
Y5
Y6B
BSEL2
72-2
73-2
74-2
YSWB[47:32]
75-3
Y4
Y5
Y6B
BSEL3
72-3
73-3
74-3
YSWB[63:48]
75-4
Y4B
Y5B
Y6
BSEL4
72-4
73-4
74-4
YSWB[79:64]
75-5
Y4
Y5B
Y6
BSEL5
72-4
73-4
74-4
YSWB[95:80]
75-6
Y4B
Y5
Y6
BSEL6
72-6
73-6
74-6
YSWB[111:96]
75-7
Y4
Y5
Y6
BSEL7
72-7
73-7
74-7
YSWB[127:112]

FIG. 5(c)

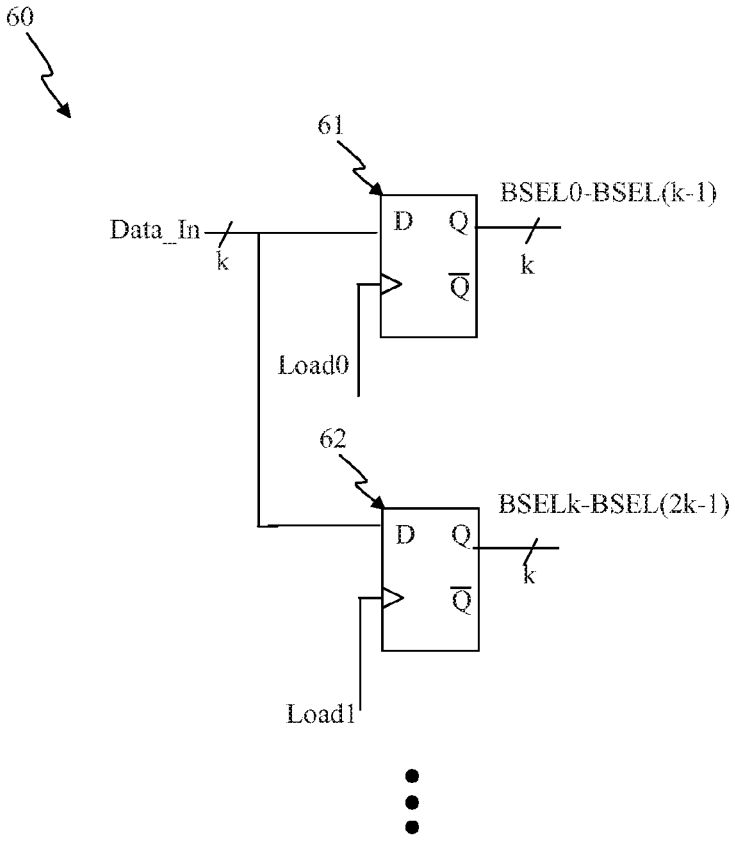
60
61
BSEL0-BSEL(k-1)
Data_In
k
D
Q
Q
k
Load0
62
BSELk-BSEL(2k-1)
D
Q
Q
k
Load1

FIG. 6

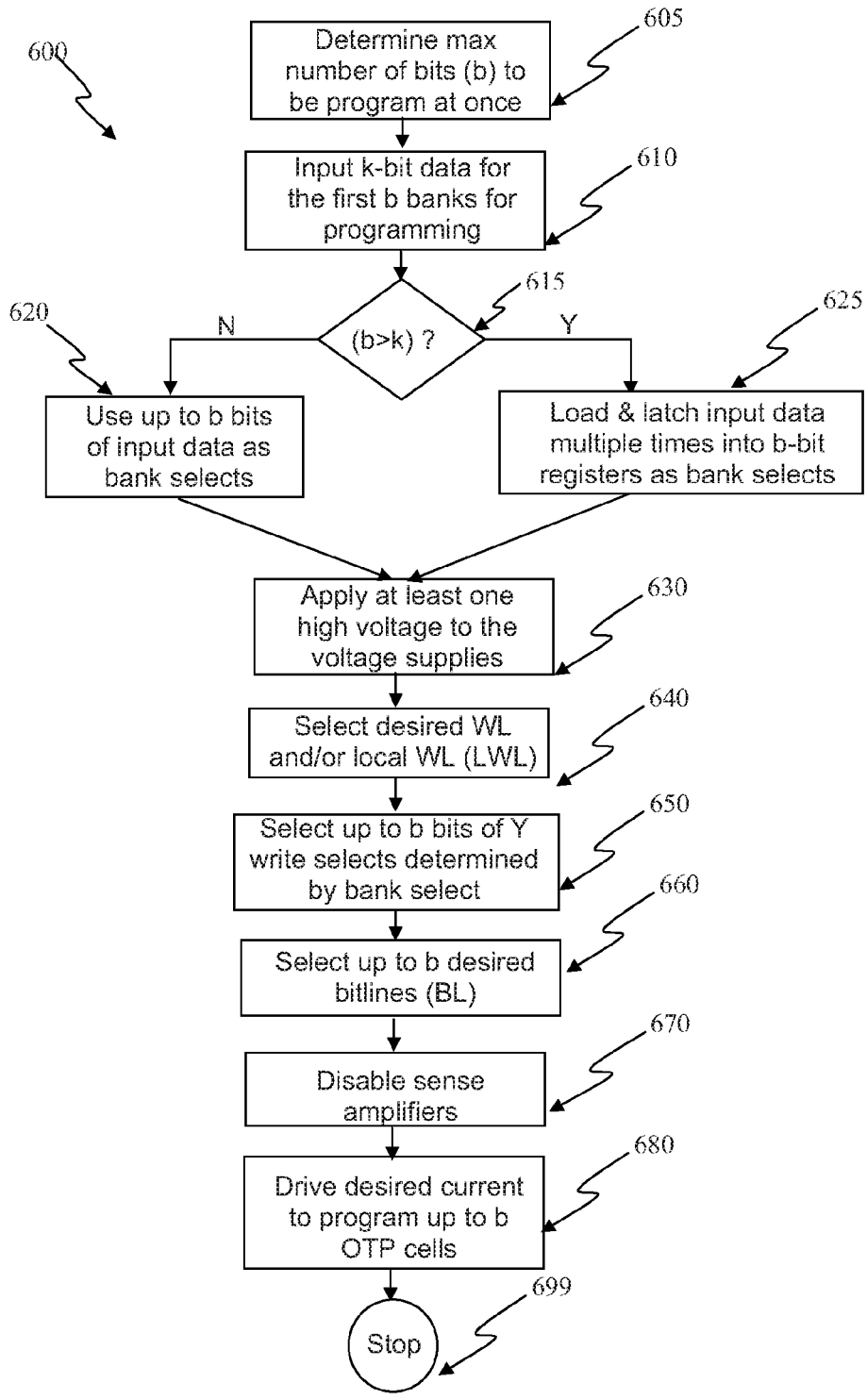
600
Determine max number of bits (b) to be program at once
605
Input k-bit data for the first b banks for programming
610
(b>k) ?
615
N
Y
620
625
Use up to b bits of input data as bank selects
Load & latch input data multiple times into b-bit registers as bank selects
Apply at least one high voltage to the voltage supplies
630
Select desired WL and/or local WL (LWL)
640
Select up to b bits of Y write selects determined by bank select
650
Select up to b desired bitlines (BL)
660
Disable sense amplifiers
670
Drive desired current to program up to b OTP cells
680
Stop
699

FIG. 7

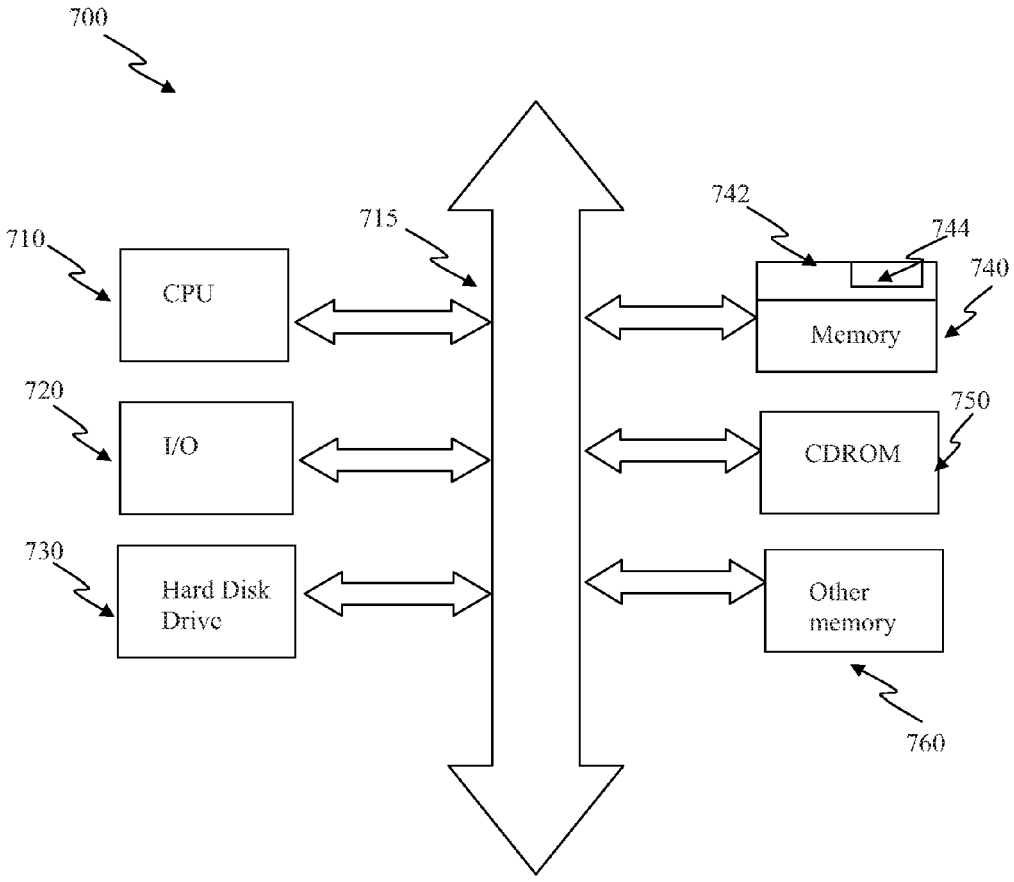
700
710
CPU
715
742
744
740
Memory
720
I/O
750
CDROM
730
Hard Disk Drive
Other memory
760

FIG. 8

CIRCUIT AND SYSTEM FOR CONCURRENTLY PROGRAMMING MULTIPLE BITS OF OTP MEMORY DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority of U.S. Provisional Patent Application No. 61/728,241 filed on Nov. 20, 2012 and entitled "CIRCUIT AND SYSTEM OF CONCURRENTLY MULTIPLE BITS PROGRAMMABLE FOR OTP MEMORY DEVICES," and is hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to programmable memory devices, particularly one-time programmable (OTP) devices, for use in memory arrays.

2. Description of the Related Art

A One-Time Programmable (OTP) device, such as electrical fuse, is a device that can be programmed only once. The programming means can apply a high voltage to induce a high current to flow through the OTP element. When a high current flows through an OTP element by turning on a program selector, the OTP element can be programmed, or burned into a high or low resistance state (depending on either fuse or anti-fuse).

An electrical fuse is a common OTP element that can be constructed from a segment of interconnect, such as polysilicon, silicided polysilicon, silicide, metal, metal alloy, or some combination thereof. The metal can be aluminum, copper, or other transition metals. One of the most commonly used electrical fuses is a CMOS gate, fabricated in silicided polysilicon or metal gate, used as interconnect. The electrical fuse can also be one or more contacts or vias instead of a segment of interconnect. A high current may blow the contact(s) or via(s) into a very high resistance state. The electrical fuse can be an anti-fuse, where a high voltage makes the resistance lower, instead of higher. The anti-fuse can consist of one or more contacts or vias with an insulator in between. The anti-fuse can also be a CMOS gate coupled to a CMOS body with a thin gate oxide as insulator.

A conventional OTP memory cell **10** is shown in FIG. **1**. The cell **10** consists of an OTP element **11** and an NMOS program selector **12**. The OTP element **11** is coupled to the drain of the NMOS **12** at one end, and to a high voltage V+ at the other end. The gate of the NMOS **12** is coupled to a select signal (Sel), and the source is coupled to a low voltage V−. When a high voltage is applied to V+ and a low voltage to V−, the OTP cell **10** can be programmed by raising the select signal (Sel) to turn on the NMOS **12**. One of the most common OTP elements is a silicided polysilicon, the same material and fabricated at the same time as a MOS gate. The size of the NMOS **12**, as program selector, needs to be large enough to deliver the required program current for a few microseconds. The program current for a silicided polysilicon is normally between a few milliamps for a fuse with width of 40 nm to about 20 mA for a fuse with width about 0.6 um. As a result, the cell size of an electrical fuse using silicided polysilicon tends to be very large. The resistive cell **10** can be organized as a two-dimensional array with all Sel's and V−'s in a row coupled as wordlines (WLs) and a ground line, respectively, and all V+'s in a column coupled as bitlines (BLs).

Another conventional OTP memory cell **15** is shown in FIG. **2**. The OTP memory cell has an OTP element **16** and a diode **17** as program selector. The OTP element **16** is coupled between an anode of the diode **17** and a high voltage V+. A cathode of the diode **17** is coupled to a low voltage V−. By applying a proper voltage between V+ and V− for a proper duration of time, the OTP element **16** can be programmed into high or low resistance states, depending on voltage/current and duration. The diode **17** can be a junction diode constructed from a P+ active region on N well and an N+ active region on the same N well as the P and N terminals of a diode, respectively. In another embodiment, the diode **17** can be a diode constructed from a polysilicon structure with two ends implanted by P+ and N+, respectively. The P or N terminal of either junction diode or polysilicon diode can be implanted by the same source or drain implant in CMOS devices. Either the junction diode or polysilicon diode can be built in standard CMOS processes without any additional masks or process steps. The OTP cells **15** can be organized as a two-dimensional array with all V+'s in the same columns coupled together as bitlines (BLs) and all V−'s in the same rows coupled together as wordline bars (WLBs).

The program current of an OTP memory, especially for fuse memory, can be easily larger than 10 mA for CMOS generation above 40 nm and the program time can be easily longer than 10 us. If an OTP memory has 256 Kb, the total program time can be up to 2.56 seconds, which is unacceptably long in today's manufacturing. Long tester time results in higher costs. Normally, testing a chip requires only about 2-3 sec. maximum. If programming an OTP memory requires more than 1 sec, the cost of a chip using OTP would be too high.

In the past, programming a fuse memory is one bit at a time. This is partly because of high programming current incurred such that programming multiple bits at the same time would need very wide power and/or ground buses to handle high current. For example, if programming a bit requires 10 mA, programming 8 bits concurrently would require 80 mA. Even a 5 ohm resistance in the power or ground buses would have voltage drop of 400 mV. This is unacceptable high, especially the supply voltage has been reduced over the years from 5 Volts (V), to 3.3 V, even to about 1.2 V. Thus, there is a need for improved techniques and designs for concurrently programming bits of an OTP memory, such as fuse memory.

SUMMARY

Embodiments of circuits and systems for programming multiple bits concurrently for an OTP memory, such as fuse memory, are disclosed. The fuse memory can be programmed with more than one bit at the same time to save program time and costs.

In one embodiment, an OTP memory can have multiple banks with each bank select to enable at least one Y-write select. The Y-write selects can be generated from Y-decoders from the Y-address inputs. The bank selects can be obtained from data input during programming or latched data input before programming. If data input is high, the bank select can be asserted so that at least one Y-write select can turn on at least one selected bitline for programming along with the turning on of at least one wordline. If data input is low, the bank select can be de-asserted so that no bitlines can be turned on for the corresponding bank. As a result, each bank can be selected or de-selected for programming independently if the data input are asserted or de-asserted, respectively, to achieve concurrent multiple bit programming. Data input can be shared with the same I/O ports as the data output ports during

read. The multiple-bit programming scheme is particularly suitable for using diodes as program selectors when the program currents can be very low. Thus, test time and costs can be reduced substantially for large density OTP memories.

Embodiments of the invention can be implemented in numerous ways, including as a method, system, device, or apparatus (including graphical user interface and computer readable medium). Several embodiments of the invention are discussed below.

As an OTP memory, one embodiment can, for example, include a plurality of One-Time Programmable (OTP) cells in a multiple-bank OTP memory. Each bank can have a plurality of wordlines, or the complements, that can be selected during programming. Each bank can also have a plurality of bitlines that can be selected by enabling at least one bank select signal and bitline selects during programming. The wordlines (or the complements), and the bitlines can be generated from the X- and Y-decoders from the X and Y address inputs, respectively. If a bank select is asserted, at least one bitline can be selected for programming, along with at least one selected wordlines (or complements). The bank select signals can be obtained from the data input, which can share the same I/O ports as data output during read. If the number of bits to be concurrently programmed is larger than the width of the I/O ports, the data input can be loaded and latched multiple times as bank selects.

As an electronics system, one embodiment can, for example, include at least a processor, and an OTP memory operatively connected to the processor. The OTP memory can include at least a plurality of OTP cells within multiple banks for data storage. Each bank can have a plurality of wordlines, or complements, that can be selected during programming. Each bank can also have a plurality of bitlines that can be selected by enabling at least one bank select and at least one bitline during programming. The wordlines (or the complements), and the bitlines can be generated from the X- and Y-decoders from the X and Y address inputs, respectively. If a bank select is asserted, at least one bitline can be selected from the corresponding bank for programming along with at least one selected wordlines (or complements). As a result, each bank can be asserted or de-asserted for programming, depending on the bank select to achieve concurrent multiple-bit programming. The bank selects can be obtained from data input during programming or latched data input before programming. Data input for bank select can be shared with the same I/O ports as data output during read. The multiple-bit programming scheme is particularly suitable for using diodes as program selectors when the program current can be very low. Thus, test time and costs can be reduced substantially for large density OTP memories.

As a method for providing a concurrent multiple-bit programmable One-Time Programmable (OTP) memory, one embodiment can, for example, include at least providing an OTP memory with a plurality of OTP cells, and concurrently programming a logic state into at least one of the OTP cells by turning on at least one selected wordline (or complement) and at least one of the bitline in at least one bank. The concurrent multiple-bit programming OTP can include at least (i) a multiple-bank OTP cell array that has a plurality of wordlines (or complements) and a plurality of bitlines to be selected, (ii) a plurality of bank selects to enable turning on at least one selected bitlines in a plurality of banks so that a plurality of OTP cells can be programmed concurrently, if at least one wordline is also turned on, and (iii) a scheme to input data as the bank selects. The bank selects can be input and/or latched from the I/O ports by sharing the same I/O ports with data output during read.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed descriptions in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

FIG. **1** shows a conventional OTP cell using MOS as a program selector in a prior art.

FIG. **2** shows another conventional OTP cell using diode as a program selector.

FIG. **3** shows a block diagram of a portion of concurrent multi-bit programmable OTP memory according to one embodiment.

FIG. **4** shows a schematic of a portion of one bank in an OTP memory according to one embodiment.

FIG. **5**(*a*) shows a block diagram of a Y-decoder block with a bank select according to one embodiment.

FIG. **5**(*b*) shows a portion of Y decoder block that has a plurality of Y address buffers, Y pre-decoders, and Y-decoders according to one embodiment.

FIG. **5**(*c*) shows a portion of an exemplifying Y decoder block according to another embodiment.

FIG. **6** shows a portion of a schematic diagram to latch data input as bank selects according to one embodiment.

FIG. **7** depicts a method of programming multiple bits in an OTP memory concurrently according to one embodiment.

FIG. **8** shows a processor system including at least one multi-bit concurrently programmable OTP memory according to one embodiment.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Circuits and systems for concurrently programming a plurality of OTP cells in an OTP memory are disclosed. An OTP memory can have a plurality of OTP cells. Each OTP cell can have an electrical fuse element coupled a program selector. The program selector can have a control terminal. The control terminals of a plurality of OTP cells can be coupled to a plurality of local wordlines that have a first resistivity. A plurality of the local wordlines can be coupled to at least one global wordline that has a second resistivity. A plurality of banks of bitlines that can have each bitline coupled to a plurality of the OTP cells via the control terminal of the program selector. A plurality of bank selects can enable turning on the wordlines or bitlines in a bank. A plurality of the OTP cells can be configured to be programmable concurrently into a different logic state by applying voltages to at least one selected global wordlines and at least one selected bitlines to a plurality of the selected OTP cells in a plurality of banks, if a plurality of bank selects are asserted.

The program selector can be a MOS device or a junction diode fabricated from a standard CMOS technology. The OTP element can be polysilicon, silicided polysilicon, silicide, polymetal, metal, metal alloy, local interconnect, metal-0, thermally isolated active region, CMOS gate, or combination thereof.

Embodiments disclosed herein can use a plurality of bank selects to enable each bank independently for concurrent multiple-bit programming. A multiple-bank OTP memory can have a plurality of wordlines (or complements) and a plurality of bitlines for a plurality of banks. The wordlines or bitlines can be generated from the X- and Y-decoders from the X and Y address inputs, respectively. If bank selects for a plurality of banks are asserted, at least one bitline can be selected from the plurality of banks, along with at least one wordline can be selected, to implement programming. The

bank selects can be obtained from data inputs and can share the same I/O port with data output during read. The bank selects can be latched from data inputs multiple times before programming.

Several embodiments of the invention are discussed below with reference to FIGS. **3-8**. However, those skilled in the art will readily appreciate that the detailed description given herein with respect to these figures is for explanatory purposes as the invention extends beyond these limited embodiments.

FIG. **3** shows a block diagram of a portion of a multiple-bit concurrently programmable OTP memory **30** according to one embodiment. The OTP memory **30** has at least one OTP memory array **31** that has b banks of OTP memory **31-0** through **31**-(b−1). X decoder block **32** generates n rows of wordlines (or complements) to be selected for at least one row in the OTP memory array **31** for programming. Y decoder block **33** generates m columns of bitlines to be selected for at least one column in at least one bank for programming. Data_In_MUX **34** generates a set of b bank selects, BSEL0 through BSEL(b−1), from k bits of data input (Data_In). If the number of the bank selects is not more than the width of the data input, the data input in part or all can be used as bank selects. If the number of the bank selects is larger than width of the data input, the data can be input several times and latched as bank selects. The bank selects can further undergo a logical AND with the m column selects from the Y decoder block **33** outputs in gates **35-0** through **35**-(m−1) to enable selecting at least one bitline in a bank independently. For example, if all bank selects, BSEL0-BSEL(b−1), are asserted, a column specified by the m bits of the Y-decoder block **33** output of all banks can be programmed at the same time, if at least one wordline is also selected. Similarly, if only BSEL0 is asserted, but all the other bank selects are de-asserted, only bank 0 can be programmed to at least one bitline specified by the Y decoder block **33** output, if at least one wordline is also selected.

The above discussions are for illustrative purposes. The number of cells may vary. The numbers of rows n, columns m per bank, banks b, or data bus width k may vary. The number of banks and the number of bits to be programmable concurrently are not necessarily the same, though it is more convenient to do so. The row and column can be interchangeable. The AND gates, **35-0** through **35**-(b−1), can be built as part of the Y-decoder block **33** to be functional equivalent to enable at least one bitline from at least one bank, if the corresponding bank select is asserted. The numbers of bits that can be programmed concurrently may vary for each programming cycle depending on how many bank selects are asserted, as long as they do not exceed a maximum number b, in the above example. There are many variations and equivalent embodiments and that they are all within the scope of this invention for those skilled in the art.

FIG. **4** shows a portion of a schematic diagram of a portion of an OTP memory bank **100** according to one embodiment. The OTP memory bank **100** can be constructed by an array **101** of n-row by m-column using diode-as-program-selector cells **110** and n wordline drivers **150**-i, where i=0, 1, . . . , n−1, in accordance with one embodiment. The memory array **101** has m columns to be selected for programming. Each of the memory cells **110** has an OTP element **111** coupled to the P terminal of a diode **112** as program selector and to a bitline BLj **170**-j (j=0, 1, . . . m−1) for those of the memory cells **110** in the same column. The N terminal of the diode **112** is coupled to a wordline WLBi **152**-i through a local wordline LWLBi **154**-i, where i=0, 1, . . . , n−1, for those of the memory cells **110** in the same row. Each wordline WLBi is coupled to at least one local wordline LWLBi, where i=0, 1, . . . , n−1. The LWLBi **154**-i is generally constructed by a high resistivity material, such as N well, polysilicon, polymetal, local interconnect, metal-0, active region, or metal gate to connect cells, and then coupled to the WLBi (e.g., a low-resistivity metal WLBi) through conductive contacts or vias, buffers, or post-decoders **172**-i, where i=0, 1, . . . , n−1. Buffers or post-decoders **172**-i may be needed when using diodes as program selectors because there are currents flowing through the WLBi, especially when one WLBi drives multiple cells for program simultaneously in other embodiments. The wordline WLBi is driven by the wordline driver **150**-i with a supply voltage vddi that can be switched between different voltages for program and read. Each BLj **170**-j is coupled to a supply voltage VDDP through a Y-write pass gate **120**-j for programming, where each BLj **170**-j is selected by YSWBj (j=0, 1, . . . , m−1). The Y-write pass gate **120**-j (j=0, 1, . . . , m−1) can be built by PMOS, though NMOS, diode, or bipolar devices can be employed in some embodiments. To program a cell, the specific WLBi and YSWBj can be turned on to select a wordline and a bitline, respectively, when a high voltage is supplied to VDDP, where i=0, 1, . . . n−1 and j=0, 1, . . . , m−1. Thus, an OTP memory cell can be programmed into a desirable state. For those skilled in the art understand that the above descriptions are for illustrative purpose. Various embodiments of array structures, configurations, and circuits are possible and are still within the scope of this invention.

FIG. **5**(*a*) shows a portion of an Y decoder block **40**, corresponding to the Y decoder block **33** and AND gates **35**-i (i=0, 1, 2, . . . , m−1) in FIG. **3**, according to another embodiment. The Y decoder block **40** consists of a plurality of Y decoders enabled by a bank select (BSELi) to generate Y Write Selects YSWB0-YSWB(m−1) for bank i with a plurality of Y address (Y ADDR) inputs, where i=0, 1, . . . , b−1. The Y decoder block can be replicated for the other banks, though some of the circuits can be shared.

FIG. **5**(*b*) shows a portion of an Y decoder block **50**, corresponding to the Y decoder block **40** in FIG. **5**(*a*), according to one embodiment. The Y decoder block **50** has at least one Y address buffer **57**, at least one Y pre-decoder **58**, and at least one Y decoder **59**. The Y address buffer **57** has at least one input from Y address (YADDR) to generate true and complement of Y addresses, YA and YAB, through buffers **51-1** and **51-2**, and **51-3**, respectively. The Y pre-decoder **58** has at least one multiple-input NAND **52-1** followed by an inverter as a buffer **52-2**. The NAND **52-1** can have at least one input from the buffered Y address and a bank select BSELi, i=0, 1, . . . , b−1. The Y decoder **59** has at least one multiple-input NAND **53-1** and followed by none, one , , , or a suitable number of buffers to generate Y-Write Selects YSWB0-YSWB(m−1). The bank select BSELi can be gated with the Y address in the Y address buffer **57**, or in the Y decoder **59**, in other embodiments. The Y address buffers can be replicated for as many times as the Y address inputs. The outputs of the buffered Y addresses can be input to a plurality of Y pre-decoders **58** to pre-decoder the Y address space partially. Furthermore, the outputs of the Y pre-decoders **58** can be input to a plurality of Y decoders **59** to fully decode the available Y addresses. In this example, there are m*b YSWB signals to be generated from the Y decoder block **50** for m columns in b banks, and up to b YSWB signals can be asserted, one for each bank.

The X decoder block **32** in FIG. **3** can be implemented similarly to the Y decoder block **50** in FIG. **5**(*b*) in other embodiment, except that the BSELi can be changed into a single or a plurality of wordline enables. More generally, the number of inputs and stages of multiple-input NAND gates

may vary, depending on the number of the Y addresses and pre-decoding/decoding schemes. The NAND gates can be replaced by equivalent NOR gates or equivalent Boolean logic in other embodiments. The numbers of buffers may vary. In other embodiments, the number of banks and the maximum number of bits that can be programmed concurrently do not have to be the same, thought it is more convenient to design this way.

FIG. **5**(*c*) shows a portion of an exemplifying Y decoder block **70** according to another embodiment. The Y decoder block **70** can fully decode into 128 Y select lines from 7 Y addresses for an OTP memory. The OTP memory has 8 banks, 0 to 7, that can be decoded from the upper 3 Y addresses Y5, Y6, and Y7, in the increment order. A Y pre-decoder **71** has a 4-input NAND **71-1** with inputs from Y0-Y3 address buffers and followed by an inverter **71-2** as a buffer. Another pre-decoder block **72-0** has a 3-input NAND **76-0** with inputs from Y4B, Y5B, and Y6B and another inverter **73-0** with bank select BSEL0 as input. The outputs of the gates **76-0** and **73-0** are inputs to an NOR **74-0** to generate a bank select output. The pre-decoder outputs of Y0B, Y1B, and Y2B are combined with the bank select output to generate 16 Y-write selects 15 through 0 in a two-input NAND **75-0**. The Y-write selects from 16 to 127 for bank 1 through 7 can be generated similarly in the other gates **76**-i, **73**-i, **74**-i, and **75**-i, respectively, where i=1, 2, 3, . . . 7. By asserting a plurality of bank selects, BSLE0-BSEL7, a plurality of Y-write selects YSWBs can be selected, at most one in each bank. As a consequence, a plurality of bitlines can be selected for concurrent multiple-bit programming, if at least one wordline is also selected.

FIG. **6** shows a portion of a schematic diagram of a data input mux **60** as Data_In_MUX shown in FIG. **3** according to one embodiment. The Data_In_MUX is a circuit block for generating bank select signals based on the data input from I/O ports, especially when the numbers of bits to be programmed concurrently are larger than the I/O port width. The Data_In_MUX can have as many inputs as the width of the I/O ports for Data_In. Each Data_In signal can be coupled to at least one latch or register **61** for bank selects. When a load signal, Load**0**, is asserted, the input data Data_In can be latched into the latches or registers **61** as bank selects from BSEL0 to BSEL(k−1), if k is the width of the I/O ports. Similarly, the bank selects from BSELk to BSEL(2k−1) can be latched into latches or registers **62** by asserting another load signal Load**1** subsequently. This process can continue until all bank selects are loaded with proper values. These values can determine the corresponding banks being programmed or not in the next programming cycle. The processes of loading bank selects can be performed before each programming cycle. If the width of the I/O ports k is larger than the numbers of bits to be programmed concurrently, the latches or register can be omitted in other embodiments.

The OTP memory in the above discussions can include many different types of OTP elements. The OTP element can be an electrical fuse including a fuse fabricated from an interconnect, contact/via fuse, contact/via anti-fuse, or gate oxide breakdown anti-fuse. The interconnect fuse can be formed from silicide, polysilicon, silicided polysilicon, poly-metal, metal, metal alloy, local interconnect, metal-0, thermally insulated active region, or some combination thereof, or can be constructed from a CMOS gate. For the electrical fuse fabricated from an interconnect, contact, or via fuse, programming requirement is to provide a sufficiently high current, about 4-20 mA range, for a few microseconds to blow the fuse by electro-migration, heat, ion diffusion, or some combination thereof. For anti-fuse, programming requirement is to provide a sufficiently high voltage to breakdown the dielectrics between two ends of a contact, via or CMOS gate/body. The required voltage is about 6-7V for a few millisecond to consume about 100 uA of current for an OTP cell in today's technologies.

The OTP memory in the above discussions can include many different types of program selectors. The program selectors can be at least a MOS device that can be either NMOS or PMOS in bulk or SOI CMOS, in planar or FinFET technologies. The drain of the MOS device can be coupled to the OTP element and the gate of the MOS device can be coupled to a wordline. The program selector can also be a diode having at least a first active region with a first type of dopant to provide a first terminal of the diode, and an isolated second active region with a second type of dopant to provide a second terminal of the diode, both active regions being fabricated from sources or drains of CMOS devices and residing in a common CMOS well, the first terminal of the diode coupled to a first terminal of the OTP element and the second terminal of the diode can be coupled to a wordline complement. The isolation between the first and the second active region can be via STI, LOCOS, dummy MOS gate, or silicide block layer.

FIG. **7** depicts a flow diagram of a method **600** for programming a multi-bit programmable OTP memory in accordance with one embodiment. In the first step **605**, determine a maximum number of bits, b, to be programmed concurrently. In the step **610**, input k-bit data from I/O ports as bank selects. In the step **615**, compare the number of bits b to be concurrently programmed with the width of the I/O ports k. If the number of bits to be programmed concurrently is not more than the width of the I/O ports, just use up to b bits in the I/O ports as bank selects in step **620**. If not, load and latch the k-bit input data from the I/O ports multiple times until all bank select registers have been updated in step **625**. Then apply at least one high voltage as voltage supplies for programming in step **630**. The next step is to select the at least one desired wordline (WL) and local wordline (LWL) to select at least one row in step **640**. Then select up to b bits of the Y write selects determined by the bank selects in step **650** where the bank selects were input or latched from the I/O ports. After Y write selects are asserted, up to b columns of bitlines can be selected for programming in step **660**. The sense amplifiers for read can be disabled in step **670** to save power and to avoid interfering with the program operation. Finally, proper currents can be driven to a plurality of OTP cells, up to b OTP cells, selected for programming concurrently in step **680**. Then, the process of programming multiple bits concurrently stops in **699** until the next programming cycle.

FIG. **7** shows a flow chart depicting embodiments of a program method **600** for concurrently programming multiple bits of a programmable OTP memory in accordance with certain embodiments. The method **600** is described in the context of a One-Time Programmable (OTP) memory, and more particularly a fuse memory, such as the OTP memory block **100** in FIG. **4**. In addition, although described as a flow of steps, one of ordinary skilled in the art will recognize that at least some of the steps may be performed in a different order, including simultaneously, or skipped.

FIG. **8** shows a processor system **700** according to one embodiment. The processor system **700** can include at least one OTP device **744**, such as in a cell array **742**, in multiple-bit concurrently programmable OTP memory **740**, according to one embodiment. The processor system **700** can, for example, pertain to a computer system. The computer system can include a Central Process Unit (CPU) **710**, which communicate through a common bus **715** to various memory and peripheral devices such as I/O **720**, hard disk drive **730**,

CDROM **750**, memory **740**, and other memory **760**. Other memory **760** is a conventional memory such as SRAM, DRAM, or flash, typically interfaces to CPU **710** through a memory controller. CPU **710** generally is a microprocessor, a digital signal processor, or other programmable digital logic devices. Programmable OTP Memory **740** is preferably constructed as an integrated circuit, which includes the memory array **742** having at least one OTP device **744**. If desired, the memory **740** may be combined with the processor, for example CPU **710**, in a single integrated circuit.

The invention can be implemented in a part or all of an integrated circuit in a Printed Circuit Board (PCB), or in a system. The OTP memory can be a fuse memory such as interconnect fuse, contact fuse, or via fuse. The fuse can be silicided or non-silicided polysilicon fuse, thermally insulated active-region fuse, local interconnect fuse, metal-0 fuse, metal fuse, contact fuse, via fuse, or fuse constructed from CMOS gates. The contact or via fuse can be a single or a plurality of contact or via to be programmed into a high resistance state.

This application also incorporates by reference the following: (i) U.S. patent application Ser. No. 13/471,704, filed on May, 15, 2012 and entitled "Circuit and System of Using Junction Diode as Program Selector For One-Time Programmable Devices," which is hereby incorporated herein by reference; (ii) U.S. patent application Ser. No. 13/026,752, filed on Feb. 14, 2011 and entitled "Circuit and System of Using Junction Diode as Program Selector for One-Time Programmable Devices," which is hereby incorporated herein by reference; (iii) U.S. Provisional Patent Application No. 61/375,653, filed on Aug. 20, 2010 and entitled "Circuit and System of Using Junction Diode As Program Selector for Resistive Devices in CMOS Logic Processes," which is hereby incorporated herein by reference; (iv) U.S. Provisional Patent Application No. 61/375,660, filed on Aug. 20, 2010 and entitled "Circuit and System of Using Polysilicon Diode As Program Selector for Resistive Devices in CMOS Logic Processes," which is hereby incorporated herein by reference; and (v) U.S. patent application Ser. No. 13/026,656, filed on Feb. 14, 2011 and entitled "Circuit and System of Using Polysilicon Diode As Program Selector for One-Time Programmable Devices," which is hereby incorporated herein by reference;

The above description and drawings are only to be considered illustrative of exemplary embodiments, which achieve the features and advantages of the present invention. Modifications and substitutions of specific process conditions and structures can be made without departing from the spirit and scope of the present invention.

The many features and advantages of the present invention are apparent from the written description and, thus, it is intended by the appended claims to cover all such features and advantages of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation as illustrated and described. Hence, all suitable modifications and equivalents may be resorted to as falling within the scope of the invention.

What is claimed is:

1. An One-Time Programmable (OTP) memory capable of multiple-bit programming, comprising:

a plurality of OTP cells, at least one of the OTP cells including an electrical fuse element coupled to a program selector, the program selector having a control terminal;

a plurality of local wordlines, each coupled to a plurality of the OTP cells via the control terminal of the program selector and having a first resistivity;

a plurality of global wordlines, each coupled to at least one of the local wordlines and having a second resistivity; and

a plurality of banks of bitlines, each bitline coupled to a plurality of the OTP cells;

a plurality of bank selects to enable turning on the wordlines or bitlines in a bank; and

wherein a plurality of OTP cells can be configured to be concurrently programmable by applying at least one voltage to at least one wordline and at least one bitline in a plurality of banks if a plurality of the bank selects are asserted.

2. An OTP memory as recited in claim **1**, wherein the electrical fuse element is at least one of an interconnect, a conductive contact or via, or combination thereof.

3. An OTP memory as recited in claim **2**, wherein the electrical fuse element has at least one of polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, metal-0, thermally insulated active region, metal, or metal alloy, CMOS gate, or combination thereof.

4. An OTP memory as recited in claim **1**, wherein the at least one of the bank selects is driven from an I/O port that also serves as a data output port during read.

5. An OTP memory as recited in claim **1**, wherein the at least one of the bank select is latched from an I/O port that also serves as a data output port during read.

6. An OTP memory as recited in claim **1**, wherein the program selector is at least one MOS device with the MOS gate as the control terminal.

7. An OTP memory as recited in claim **1**, wherein the program selector comprises at least one diode having at least a first active region with a first type of dopant to provide a first terminal of the diode, and a second active region with a second type of dopant to provide a second terminal of the diode, both active regions being fabricated from sources or drains of CMOS devices and residing in a common CMOS well, the first terminal of the diode coupled to a first terminal of the electrical fuse element, and the second terminal of the diode is the control terminal.

8. An OTP memory as recited in claim **1**, wherein the local wordline is at least partially formed from at least one CMOS well.

9. An OTP memory as recited in claim **1**, wherein the global wordline is constructed of metal.

10. An OTP memory as recited in claim **1**, wherein the global wordline is coupled to the local wordline through at least one of conductive via or contact.

11. An OTP memory as recited in claim **1**, wherein the OTP memory further comprises:

a plurality of write bitline selectors to select at least one of the bitlines coupled to a first supply voltage line; and

a plurality of wordline drivers to select at least one of the local wordlines coupled to a second supply voltage line to conduct currents through a plurality of the OTP cells during programming.

12. An One-Time Programmable (OTP) memory capable of concurrent multi-bit programming, comprising:

a plurality of OTP cells, each of the OTP cells including (i) an electrical fuse element as an OTP element, and (ii) a diode as program selector having at least a first active region with a first type of dopant to provide a first terminal of the diode, and a second active region with a second type of dopant to provide a second terminal of the diode, both active regions being fabricated from sources

or drains of CMOS devices and residing in a common CMOS well, the first terminal of the diode coupled to a first terminal of the OTP element;

a plurality of local wordlines, each coupled to a plurality of the OTP cells via the second terminal of the diodes;

a plurality of global wordlines, each coupled to at least one of the local wordlines; and

a plurality of bitlines arranged in banks, each bitline coupled to a plurality of the OTP cells via a second terminal of the OTP element; and.

wherein a plurality of OTP elements being configured to be concurrently programmable by applying at least one voltage to at least one wordline and at least one bitline coupled to a plurality of the OTP cells in a plurality of the banks.

13. An OTP memory as recited in claim **12**, wherein the electrical fuse element has at least one of polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, metal-0, thermally insulated active region, metal, or metal alloy, CMOS gate, or combination thereof.

14. An OTP memory as recited in claim **12**, wherein the OTP memory further comprises a plurality bank selects that enable turning on the wordlines or bitlines in a bank, and wherein the at least one of the bank selects is driven or latched from an I/O port that also serves as a data output port during read.

15. An OTP memory as recited in claim **12**, wherein the local wordline is at least partially formed of CMOS well and/or the global wordline is constructed of metal.

16. An electronics system, comprising:

a processor; and

at least one multiple-bit concurrently programmable OTP memory operatively connected to the processor, the OTP memory comprising:

a plurality of OTP cells, each including an electrical fuse element coupled to a program selector, the program selector having a control terminal;

a plurality of local wordlines, each coupled to a plurality of the OTP cells via the control terminal of the program selector;

a plurality of global wordlines, each coupled to at least one of the local wordlines; and

a plurality of bitlines arranged in banks, each bitline coupled to a plurality of OTP cells in a bank;

a plurality of bank selects to enable turning on the wordlines or bitlines in a bank; and

wherein a plurality of OTP cells can be configured to be concurrently programmable by applying at least one voltage to at least one wordline and at least one bitline in a plurality of the banks if a plurality of the bank selects corresponding to the plurality of the banks are asserted.

17. A method for operating a programmable OTP memory, comprising:

providing a plurality of OTP cells, each including an electrical fuse element coupled to a program selector, the program selector having a control terminal;

providing a plurality of local wordlines, each coupled to a plurality of the OTP cells via the control terminal of the program selector;

providing a plurality of global wordlines, each coupled to at least one of the local wordlines;

providing a plurality bitlines arranged in banks, each bitline coupled to a plurality of the OTP cells; and

concurrently programming a plurality of selected OTP cells into a different logic state by applying voltages to at least one selected global wordlines and at least one selected bitlines in a plurality of the banks to conduct currents and change the resistance of the selected OTP cells.

18. A memory as recited in claim **17**, wherein the electrical fuse element is at least one of an interconnect, a conductive contact or via, or combination thereof.

19. A memory as recited in claim **17**, wherein the electrical fuse element has at least one of polysilicon, silicided polysilicon, silicide, polymetal, local interconnect, metal-0, thermally insulated active region, metal, or metal alloy, CMOS gate, or combination thereof.

20. A memory as recited in claim **17**, wherein the at least one of the bank select is driven or latched from the I/O ports sharing with at least one data output port during read.

21. A memory as recited in claim **17**, wherein the program selector is at least one MOS device with the MOS gate as a control terminal.

22. A memory as recited in claim **17**, wherein the program selector is at least one diode having at least a first active region with a first type of dopant to provide a first terminal of the diode, and a second active region with a second type of dopant to provide a second terminal of the diode, both active regions being fabricated from sources or drains of CMOS devices and residing in a common CMOS well, the first terminal of the diode coupled to a first terminal of the electrical fuse element, the second terminal of the diode is a control terminal.

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